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| **National University of Computer and Emerging Sciences, Lahore Campus** | | | | |
| C:\Users\saif\AppData\Local\Microsoft\Windows\Temporary Internet Files\Content.Word\final design.jpg | **Course Name:** | **Digital Logic Design** | **Course Code:** | **EE227** |
| **Program:** | **BCS & BDS** | **Semester:** | **Spring 2022** |
| **Duration:** | **30 Minutes** | **Total Marks:** | **20** |
| **Paper Date:** | **09-June-22** | **Weight** |  |
| **Section:** | **ALL** | **Page(s):** | **3** |
| **Exam Type:** | **Final Part I Objective** |  |  |
| **Student : Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Roll No.\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section:\_\_\_\_\_\_\_** | | | | |
| **Instruction/Notes:** | * *This part consists of 20 questions only.* * *Attempt all questions on THIS PAPER.* * *In MCQs, encircle the correct option, no cutting or overwriting is allowed!* * *Once done, hand over this part to the invigilator.* * *Make sure you have written your Roll No, Name and Section on Top.* * ***Use of calculator is not allowed.*** | | | |

**(i)** (600)10 = **(1130) 8**

**(ii)** (400)8 + (9A) 16 = **(410) 10**

**(iii)** How many different numbers can a 5-bit binary word represent? **32**

**(iv**) A helpful analogy for a shift register is a *conveyor belt*. Examine this illustration showing a single conveyor belt at four different times, and determine which of the following shift register operations the sequence represents:

**Logo

Description automatically generated with medium confidence**

1. **Parallel-in, serial-out**
2. Parallel-in, parallel-out
3. Serial-in, serial-out
4. Serial-in, parallel-out

**(v)** What will be 8-bit binary representation of number 1110 having parity at most significant bit, following Even Parity? **10001110**

**(vii)** Given the numbers (1000100)2, (1000003)8, (1000002)10, (1000001)16:

|  |  |
| --- | --- |
| 1. They all have the same value | 1. (1000002)10 is the smallest |
| 1. **(1000001)16 is the biggest** | 1. None of above E. All of above |

**(viii)** Which of the following describes the operation of a positive edge-triggered JK-type flip-flop?

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| --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | 1. **If both inputs are HIGH, the output will flip.** | 1. The output will follow the input on 1 to 0 transition of clock. | | 1. When both inputs are LOW, an invalid state exists. | 1. None of above | |  |

**(ix)** What are the contents of the circular shift left register (assume initially 1010 stored).

Assume 3 clock pulses are used.

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| --- | --- | --- | --- |
| 1. **0101** | 1. 1111 | 1. 0111 | 1. None of above |

**(x)**  Circuits that employs memory elements in addition to gates is called

1. Combinational circuit
2. **Sequential circuit**
3. Combinational sequence

D. Logic circuit

**(xi)** Dual and complement of the Boolean expression is same for:

|  |  |  |  |
| --- | --- | --- | --- |
| 1. X + Y + Z | 1. XY + Z’ | 1. X'Y'Z' | 1. **None of above** |

**(xii)** The main difference between latch and Flip flop (FF) is

A. FF stores more bits  **B. Only 1 value of FF is changed in 1 clock cycle**

C. Latch and FF are same D. Both A & B E. None of above

**(xiii)** The output of an XOR gate is zero (0) when \_\_\_\_\_\_\_\_\_\_ I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one

1. I only B. IV only  **C. I and IV** D. II and III

**(xiv)** Parallel load transfer is done in:

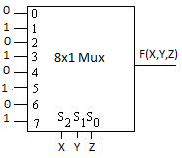
|  |  |
| --- | --- |
| 1. **1 cycle** | 1. 2 cycles |
| 1. 3 cycles | 1. 4 cycles |

**(xv)** Six bits are being used to save a number in signed 2s complement form. The range of this number will be from **(-32)**10 to **(31)**10

**(xvi)** BCD to 7-Segment is a

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1. MUX | 1. Encoder | 1. **Decoder** | 1. All of these | 1. None |

**(xvii)** If F = ∑m (0, 1, 5, 6), then F = ∏M (**2, 3, 4, 7**)

**(xviii)** An 8-line to 1-line multiplexer is connected as shown, where output is F(X, Y, Z) and Z is the least significant input. Which of the following functions does F generate?

|  |  |
| --- | --- |
| 1. F(X,Y,Z) = Z’ | 1. F(X,Y,Z) = Y |
| 1. **F (X,Y,Z) = Z** | 1. F(X,Y,Z) = Y+X |

1. None of above

**(xix)** The sequential logic circuit shown below represents most closely the basic architecture of a:

|  |  |
| --- | --- |
| 1. Data-latch register 2. Ripple counter 3. **Synchronous counter** 4. Shift register 5. None |  |

**(xx)** Identify the logic function performed by the circuit shown in the given figure:

|  |  |
| --- | --- |
| 1. 1-bit comparator 2. Full adder 3. **Half adder** 4. None of the above |  |